REMARKS

Claims 1-26 are pending in the present application. Favorable reconsideration and allowance of the application in view of the following remarks are respectfully requested.

Allowable Subject Matter

Applicant notes with appreciation that claims 5-9, 12-16, 20-21, and 24 would be allowed if rewritten in independent form including all limitations of the rejected base claims.

Status of Claim for Priority in the Application

Applicant recognizes the Examiner's acknowledgement of the claim for priority in the present application dated 1/21/2003.

Information Disclosure Statement

Applicant notes with appreciation that the Examiner has considered the references cited in the Information Disclosure Statement dated 1/20/2004, 7/5/2005, 8/3/2005, and 11/9/2005.

Claim Rejections – 35 U.S.C. § 103 Morikawa in View of Rosner

Claims 1-4, 17-19, 22, 23, and 26 stand rejected under 35 U.S.C. § 103(a) as being obvious over Morikawa et al. (US 2001/0032297) (hereinafter Morikawa) in view of Rosner et al. (US 2004/0221138) (hereinafter Rosner). Applicant respectfully traverses this art grounds of rejection.

With regard to **claim 1**, the Examiner asserts that Morikawa discloses "a first cache memory for enabling a running flag signal in response to a given interrupt signal" as recited in claim 1. Applicant asserts that the processor in Morikawa enables the target flag, rather than the

"first cache memory" enabling the target flag as recited in claim 1. Furthermore, the enablement of the target flag in Morikawa is not in response to a given interrupt signal as the Examiner asserts. In fact, the allegedly equivalent prefetch instruction is merely an "instruction that causes a data transfer to the cache memory apparatus" (paragraph [0032]) and is not an "interrupt signal."

Applicant further asserts that Morikawa neither teaches nor suggests the use of a digital signal processor (DSP) or the benefits of using such a processor in independent claim 1. The Examiner asserts that the DSP core of claim 1 reads on "Processor 1" and "naked cache." Applicant contends that not only are these two structures taught in Morikawa completely different, but the "DSP core" of claim 1 does not read on Morikawa's "naked cache" as a DSP core is designed to execute a variety of programs required for digital signal processing and performs an interrupt service routine in response to an interrupt request and Morikawa's "naked cache" is simply a data storage device. Further, Applicant contends that the "L2 Cache" 9, which is allegedly equivalent to the "first cache memory", also does not disable the flag signal.

Applicant contends that even if Rosner could be combined with Morikawa, Rosner would not remedy the deficiencies of Morikawa to make the claimed invention obvious to one skilled in the art. Therefore, Applicant respectfully requests the Examiner withdraw this art grounds of rejection.

Claims 2-4, dependent on claim 1, are patentable at least for the reasons stated above with respect to claim 1.

With regard to independent **claim 17**, the Examiner asserts that Morikawa discloses "a first cache memory ["Naked Cache" 6, Figure 1] providing a first instruction in response to a program address ["Prefetch Instruction" 31, Figure 3] received from a DSP core of the DSP

["Processor" 1, Figure 1], if there is no first instruction corresponding to the program address and outputting a first miss signal ["Cache Miss" 32, Figure 3]".

Applicant asserts that the "Naked Cache" 6 does not provide instructions but merely serves as a data storage device and therefore can not "provide a first instruction in response to a program address received from a DSP core of the DSP" as recited in claim 17. Furthermore, Applicant contends that Morikawa neither teaches nor suggests the use of a digital signal processor (DSP) or the benefits of using such a processor in claim 17. Further still, the allegedly equivalent "Processor" 1 is only taught to send address data, not receive it. Morikawa also fails to teach or suggest providing this instruction "if there is no first instruction corresponding to the program address, and outputting a first miss signal" as recited in claim 17.

For similar reasons, Applicant asserts that the "Cache-miss cache" 7 does not "provide at least one second instruction to the DSP core in response to a given interrupt signal" as recited in claim 17. Morikawa does not teach using a DSP nor sending instructions to a DSP core from a second cache memory. Further, the prefetch instruction of step 31 in Morikawa is merely an "instruction that causes a data transfer to the cache memory apparatus" (section [0032]) and is not an "interrupt signal." Further still, even if the prefetch instruction was equivalent to the "interrupt signal" of claim 17 as the Examiner suggests, the data transfer 37 does not occur in response to a prefetch instruction as illustrated in 31 of Fig. 3. Morikawa also fails to teach "the second cache memory further disabling a running flag signal based after a given number of second instructions have been provided to the DSP core" as recited in claim 17. Paragraph [0038] states: "the processor 1 sets the target flag 19 to "1". This processor of Morikawa is responsible for enabling or disabling the target flag, rather than the second cache memory.

In addition to similar reasons to those stated above with respect to the second cache memory, Applicant asserts that Morikawa's L2 Cache 9 does not provide any instruction in

response to a miss signal as is shown in Fig. 3. Steps 32 and 35 clearly show that a miss results in data being transferred to the naked cache or the cache-miss cahce. Therefore, Morikawa does not disclose "a third cache memory which provides a third instruction to the DSP core in response to the first miss signal, when the running flag signal is disabled" as recited in claim 17.

Finally, Applicant contends that combining Morikawa with the teachings of Rosner would not render the claimed invention obvious to one skilled in the art. Applicant respectfully requests the Examiner withdraw this art grounds of rejection.

Claims 18 and 19, dependent on claim 17, are patentable at least for the reasons stated above with respect to claim 17.

Independent **claim 22** includes similar limitations to those discussed above with respect to claims 1 and 17. Therefore, claim 22 is patentable at least for the reasons stated above with respect to claims 1 and 17.

Claim 23, dependent on claim 22, is patentable at least for the reasons stated above with respect to claim 22.

Claim 26 includes similar limitations to those discussed above with respect to claim 22. Therefore, claim 26 is patentable at least for the reasons stated above with respect to claim 22.

Claim Rejections – 35 U.S.C. § 103 Morikawa in View of Rosner and Chiu

Claims 10, 11, 13, and 25 stand rejected under 35 U.S.C. § 103(a) as being obvious over Morikawa et al. (US 2001/0032297) (hereinafter Morikawa) in view of Rosner et al. (US 2004/0221138) (hereinafter Rosner) and in further view of Chiu et al. (US 2001/0032297) (hereinafter Chiu). Applicant respectfully traverses this art grounds of rejection.

With regard to **claim 10**, the Examiner asserts that Morikawa discloses "(a) first providing an instruction to a DSP core of the DSP from a cache memory, in response to a request

from the DSP core" as recited in claim 10. For similar reasons to those stated above with respect to claim 1, Applicant asserts that Morikawa neither teaches nor suggests the use of a digital signal processor (DSP) or the benefits of using such a processor in independent claim 1. The Examiner asserts that the DSP core of claim 1 reads on both "Processor 1" and "naked cache." Applicant contends that not only are these two structures taught in Morikawa completely different, but the "DSP core" of claim 1 does not read on Morikawa's "naked cache" as a DSP core is designed to execute a variety of programs required for digital signal processing and performs an interrupt service routine in response to an interrupt request and Morikawa's "naked cache" is simply a data storage device.

The Examiner also asserts that Morikawa discloses "(b) enabling a running flag signal in another cache memory in response to an interrupt signal received thereto from the DSP core" as recited in claim 10. For similar reasons to those stated above with respect to claim 1, Applicant asserts that the enablement of the target flag in Morikawa is not in response to a given interrupt signal as the Examiner asserts. The "Load Instruction" from the "processor" is not equivalent to an interrupt signal from the DSP core. These are completely different signals from completely different devices.

The Examiner further asserts that the "Load Instruction" in step (c) is also equivalent to "a request from the DSP core" as well as the interrupt signal from (b). Applicant contends that these two signals are different and that neither read on "Load Instruction".

Applicant contends that even if Rosner could be combined with Morikawa, Rosner would not remedy the deficiencies of Morikawa to render independent claim 10 obvious to one skilled in the art. Furthermore, the addition of Chiu would also not remedy the deficiencies of Morikawa and Rosner. Therefore, Applicant respectfully requests the Examiner withdraw this art grounds of rejection.

Claims 11 and 13, dependent on claim 10, are patentable at least for the reasons stated above with respect to claim 10.

Claim 25 includes similar limitations to those discussed above with respect to claim 10. Therefore, claim 25 is patentable at least for the reasons stated above with respect to claim 10.

CONCLUSION

Accordingly, in view of the above amendments and remarks, reconsideration of the objections and rejections and allowance of each of claims 1-26 in connection with the present application is earnestly solicited.

Pursuant to 37 C.F.R. §§ 1.17 and 1.136(a), Applicant(s) hereby petition(s) for a one (1) month extension of time for filing a reply to the outstanding Office Action and submit the required $120 extension fee herewith.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact John A. Castellano at the telephone number of the undersigned below.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 08-0750 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

HARNESS, DICKEY, & PIERCE, P.L.C.

By: _____

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